WHAT IS CLAIMED IS:

1. A test pattern comprising:

a first metal structure disposed over a substrate;

one or more intermediate layers disposed above the first metal structure;

a second metal structure disposed above the one or more intermediate layers, wherein at least a portion of the second metal structure is above the first metal structure and the second metal structure is smaller than the first metal structure;

a first via passing through the intermediate layers and connecting the first metal structure to the second metal structure;

one or more third metal structures disposed above the one or more intermediate layers and the first metal structure, and separated from the second metal structure by a dielectric material; and

one or more second vias passing through the intermediate layers and connecting the first metal structure to the third metal structures, each second via located a predetermined radius from the center of the first via.

2. The test pattern as recited in claim 1, wherein the radius is selected to measure an effective vacancy diffusion area.

3. The test pattern as recited in claim 1, further comprising:

a fourth metal structure disposed on the substrate in close proximity to the first metal structure, wherein the one or more intermediate layers are disposed above the fourth metal structure and another portion of the second metal structure is disposed above the fourth metal structure;

a third via passing through the intermediate layers and connecting the fourth metal structure to the second metal structure;

one or more fifth metal structures disposed above the one or more intermediate layers and the fourth metal structure, and separated from the second metal structure by the dielectric material; and

one or more fourth vias passing through the intermediate layers and connecting the fourth metal structure to the fifth metal structures, each fourth via located outside of a predetermined radius from the center of the third via.

4. The test pattern as recited in claim 1, wherein the first via is approximately centered over the first metal structure.

5. The test pattern as recited in claim 1, wherein each second via is connected to a separate third metal structure.

6. The test pattern as recited in claim 1, wherein all of the second vias are connected to a single third metal structure.

7. The test pattern as recited in claim 1, wherein the intermediate layers substantially comprise a dielectric material.

8. The test pattern as recited in claim 7, wherein the dielectric material is a low-k dielectric material.

9. The test pattern as recited in claim 8, wherein the low-k dielectric material is chosen from the group consisting of polymide, silicon oxycarbide, hydrogen silsesquioxane, methyl silsesquioxane, bezocyclobutene, fluorinated glass, fluorinated aromatic ether, and inter-penetrated spin-on glass.

10. The test pattern as recited in claim 1, wherein the first metal structure, second metal structure and third metal structure comprise copper.

11. The test pattern as recited in claim 1, wherein the first via and second vias comprise copper.

12. The test pattern as recited in claim 1, wherein the radius is within a range of about 0.5 μm to about 10 μm.

13. The test pattern as recited in claim 1, wherein the first metal structure has an area selected from a range of about 100 μm2 to about 500 μm2.

14. The test pattern as recited in claim 1, wherein the first metal structure planar dimensions are about 20 μm by a multiple of about 3μm.

15. The test pattern as recited in claim 1, wherein the second metal structure and the one or more third metal structures are separated by a multiple of about 0.5 μm.

16. The test pattern as recited in claim 1, wherein:

the first metal structure planar dimensions are 20 μm by a multiple of 3μm;

the second metal structure planar dimensions are at least 0.11 μm by 10 μm;

the third metal structure planar dimensions are at least 0.3 μm by 0.3 μm;

the second metal structure and the one or more third metal structures are separated by a multiple of 0.5 μm; and

the first via and second vias have a width of at least 0.1 μm.

17. A test pattern comprising:

two or more test substructures; and

each test substructure comprising:

a first metal structure disposed on a substrate;

one or more intermediate layers disposed above the first metal structure;

a second metal structure disposed above the one or more intermediate layers, wherein at least a portion of the second metal structure is above the first metal structure and the second metal structure is smaller than the first metal structure;

a first via passing through the intermediate layers and connecting the first metal structure to the second metal structure;

one or more third metal structures disposed above the one or more intermediate layers and the first metal structure, and separated from the second metal structure by a dielectric material; and

one or more second vias passing through the intermediate layers and respectively connecting the first metal structure to the third metal structures, each second via located outside of a predetermined radius from a center of the first via, which predetermined radius is different for each test substructure.

18. The test pattern as recited in claim 17, wherein each test substructure further comprises:

a fourth metal structure disposed on the substrate in close proximity to the first metal structure;

wherein the one or more intermediate layers are disposed above the fourth metal structure and another portion of the second metal structure is disposed above the fourth metal structure;

a third via passing through the intermediate layers and connecting the fourth metal

structure to the second metal structure;

one or more fifth metal structures disposed above the one or more intermediate layers and the fourth metal structure, and separated from the second metal structure by the dielectric material; and

one or more fourth vias passing through the intermediate layers and respectively connecting the fourth metal structure to the fifth metal structures, each fourth via outside of a predetermined radius from the center of the third via.

19. The test pattern as recited in claim 17, further comprising two or more test structures, wherein each test structure comprises the two or more test substructures, and wherein the size of the first metal structure is substantially constant for each test substructure and substantially different for each test structure.

20. A method for determining an effective vacancy diffusion area for a silicon-on-insulator structure comprising the steps of:

forming two or more test substructures on the substrate, each test substructure comprising:

a first metal structure disposed on a substrate, one or more intermediate layers disposed above the first metal structure;

a second metal structure disposed above the one or more intermediate layers, wherein at least a portion of the second metal structure is above the first metal structure and the second metal structure is smaller than the first metal structure;

a first via passing through the intermediate layers and connecting the first metal structure to the second metal structure;

one or more third metal structures disposed above the one or more intermediate layers and the first metal structure, and separated from the second metal structure by a dielectric material; and

one or more second vias passing through the intermediate layers and connecting the first metal structure to the third metal structures, each second via located outside of a radius from a center of the first via, which radius is different for each test substructure;

measuring a resistance between the second metal structure and the third metal structure(s) of each test substructure before and after thermal stressing of the silicon-on-insulator structure; and

determining the effective vacancy diffusion area based on a change in the resistance measurements.

21. The method as recited in claim 20, wherein the resistance is also measured during the thermal stressing.

22. The method as recited in claim 20, wherein the thermal stressing is performed at a temperature between about 125°C and about 300°C.

23. The method as recited in claim 20, wherein the thermal stressing is performed over a duration of between about 100 and about 1000 hours.

24. The method as recited in claim 20, wherein each test substructure further comprises

a fourth metal structure disposed on the substrate in close proximity to the first metal structure;

wherein the one or more intermediate layers are disposed above the fourth metal structure and another portion of the second metal structure is disposed above the fourth metal structure;

a third via passing through the intermediate layers and connecting the fourth metal structure to the second metal structure;

one or more fifth metal structures disposed above the one or more intermediate layers and the fourth metal structure, and separated from the second metal structure by the dielectric material; and

three or more fourth vias passing through the intermediate layers and connecting the fourth metal structure to the fifth metal structures, each fourth via located outside of the radius from a center of the third via.

25. The method as recited in claim 20, wherein the first via is approximately centered over the first metal structure.